TP65H150G4PS

650V SuperGaN® GaN FET in TO-220 (source tab)

Description

The TP65H150G4PS 650V, 150mΩ Gallium Nitride (GaN) FET is a normally-off device using Renesas' Gen IV platform. It combines a state-of-the-art high voltage GaN HEMT with a low voltage silicon MOSFET to offer superior reliability and performance while enabling reduced system size and cost.

The Gen IV SuperGaN® platform uses advanced epi and patented design technologies to simplify manufacturability while improving efficiency over silicon via lower gate charge, output capacitance, crossover loss, and reverse recovery charge.

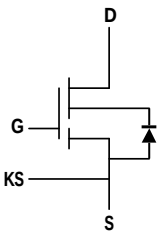
Benefits

- Achieves increased efficiency in both hard-switched and soft-switched circuits
  - Increased power density
  - Reduced system size and weight
  - Overall lower system cost
- Easy to drive with commonly used gate drivers
- GSD pin layout improves high speed design

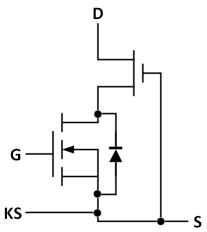
Product and Schematic Diagrams



TP65H150G4PS TO-220



Cascode Schematic Symbol



Cascode Device Structure
(MOSFET has integrated ESD Protection Circuit)

Features

- Gen IV technology
- JEDEC-qualified GaN technology
- Dynamic RDS(on)eff production tested
- Robust design, defined by:
  - Wide gate safety margin
  - Transient over-voltage capability
- Zero reverse recovery charge
- Negligible Qrr
- RoHS compliant and Halogen-free packaging

Applications

- Consumer
- Power adapters
- Low power SMPS
- Lighting

Specifications

V_{DS} (V)	650
$V_{DSS(TR)}$(V) maximum	800
$R_{DS(on)}$ (mΩ) maximum [1]	180
Q_{OSS} (nC) typical	34
Q_G (nC) typical	8

1. Dynamic $R_{DS(on)}$ (see Figure 17 and Figure 18)

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2. Specifications

2.1 Absolute Maximum Ratings

Tc = 25°C unless otherwise stated.

: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

Symbol	Parameter	Limit Value	Unit
V_{DSS}	Drain to source voltage (T_J = -55 C to 150 C)	650	V
$V_{DSS(TR)}$	Transient drain to source voltage [1]	800	
V_{GSS}	Gate to source voltage	±20	
P_D	Maximum power dissipation at T_C = 25 C	83	W
I_D	Continuous drain current at T_C = 25 C	16	A
	Continuous drain current at T_C = 100 C	10	A
I_{DM}	Pulsed drain current (pulse width: 10µs)	60	A
T_J	Operating temperature junction	-55 to +150	°C
T_S	Storage temperature	-55 to +150	°C
T_{SOLD}	Reflow soldering temperature [3]	260	°C

1. In off-state, spike duration < 30µs, non-repetitive.
2. For 10 sec., 1.6mm from the case.

2.2 Thermal Specifications

Symbol	Condition	Typical Value	Unit
$R_{\Theta JC}$	Junction-to-case	1.5	°C/W
$R_{\Theta JA}$	Junction-to-ambient	50	

1. Device on one layer epoxy PCB for source connection (vertical and without air stream cooling, with 6cm^2 copper area and 70µm thickness).

2.3 Electrical Specifications – Forward Device

T_J = 25°C unless otherwise stated.

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Unit
$V_{DSS(BL)}$	Maximum drain-source voltage	V_{GS} = 0V	650	-	-	V
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 5mA	3.3	4	4.8	V
$R_{DS(on)eff}$	Drain-source on-resistance [1]	V_{GS} = 10V, I_D = 10A, T_J = 25 C	-	150	180	mΩ
		V_{GS} = 10V, I_D = 10A, T_J = 150 C	-	307	-	
I_{DSS}	Drain-to-source leakage current	V_{DS} = 650V, V_{GS} = 0V, T_J = 25 C	-	2.5	25	µA
		V_{DS} = 650V, V_{GS} = 0V, T_J = 150 C	-	10	-	
I_{GSS}	Gate-to-source forward leakage current	V_{GS} = 20V	-	-	100	nA
	Gate-to-source reverse leakage current	V_{GS} = -20V	-	-	-100	
C_{ISS}	Input capacitance	V_{GS} = 0V, V_{DS} = 400V, *f* = 1MHz	-	598	-	pF

2.4 Electrical Specifications – Reverse Device

T_J = 25°C unless otherwise stated.

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Unit
I_S	Reverse current	V_{GS} = 0V, T_C = 100 C, ≤ 25% duty cycle	-	-	8.3	A

3. Typical Performance Graphs

T_C = 25°C unless otherwise stated.

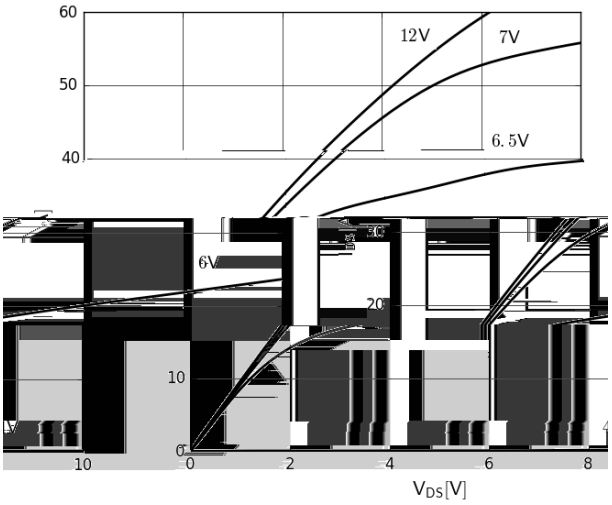


Figure 2. Typical Output Characteristics, T_J = 25°C

Parameter: V_{GS}

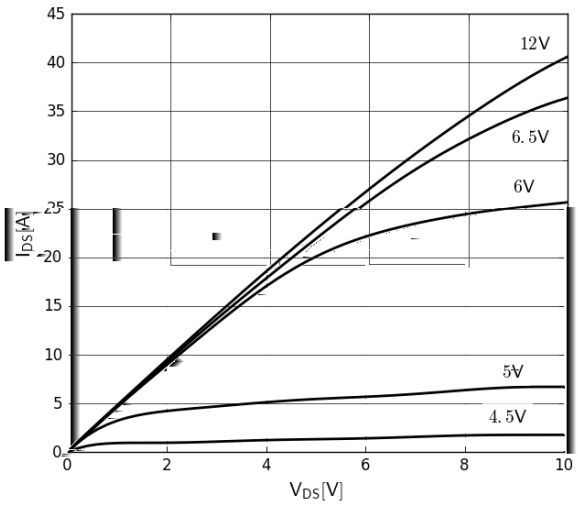


Figure 3. Typical Output Characteristics, T_J = 150°C

Parameter: V_{GS}

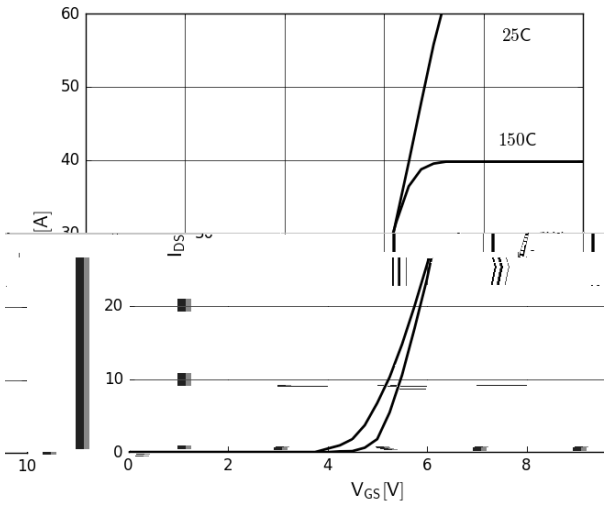


Figure 4. Typical Transfer Characteristics

V_{DS} = 10V, Parameter: T_J

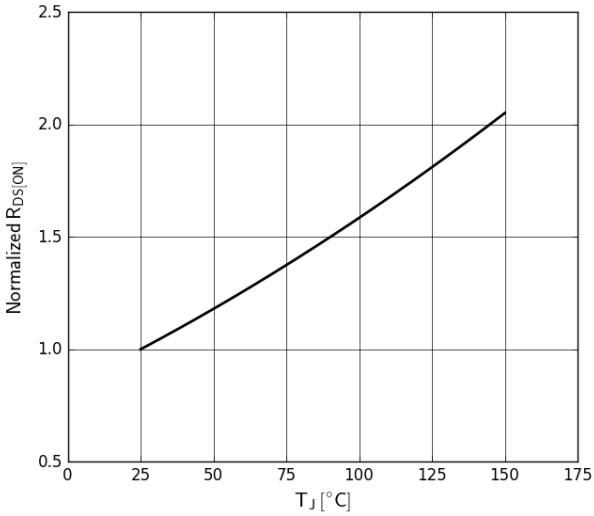


Figure 5. Normalized On-resistance

I_D = 10A, V_{GS} = 10V

Figure 10. Power Dissipation

Figure 11

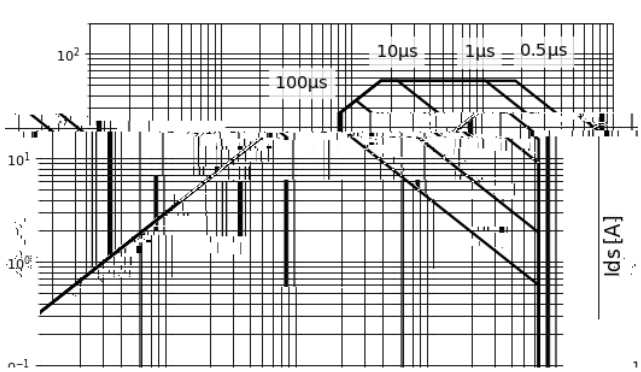


Figure 14. Safe Operating Area T_C = 25°C

4. Test Circuits and Waveforms

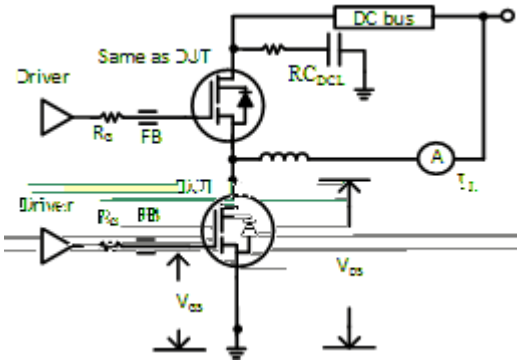


Figure 15. Switching Time Test Circuit

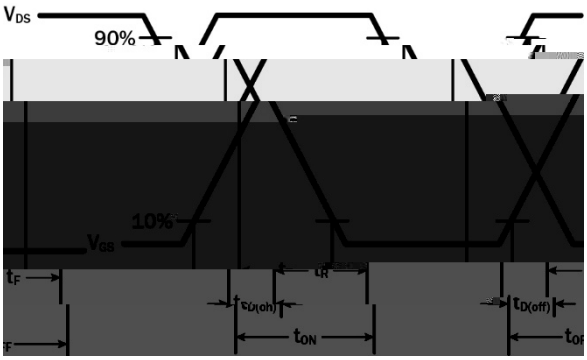


Figure 16. Switching Time Waveform

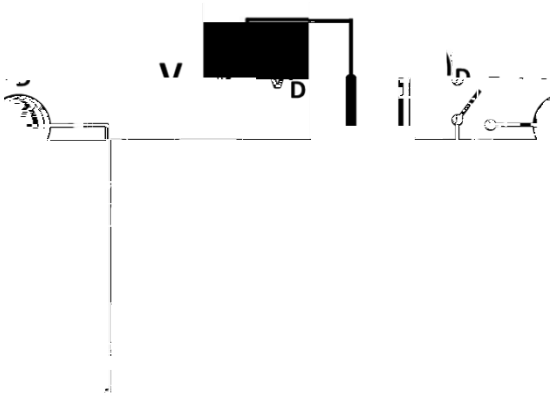


Figure 17. Dynamic $R_{DS(on)eff}$ Test Circuit

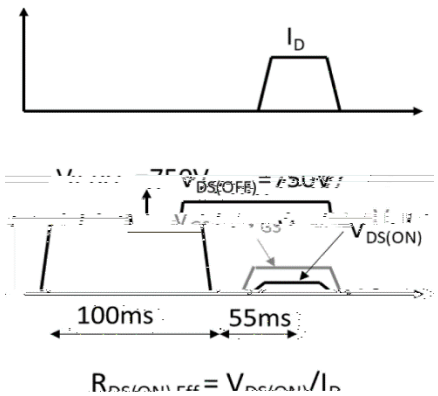


Figure 18. Dynamic $R_{DS(on)eff}$ Waveform

5. Package Outline Drawings

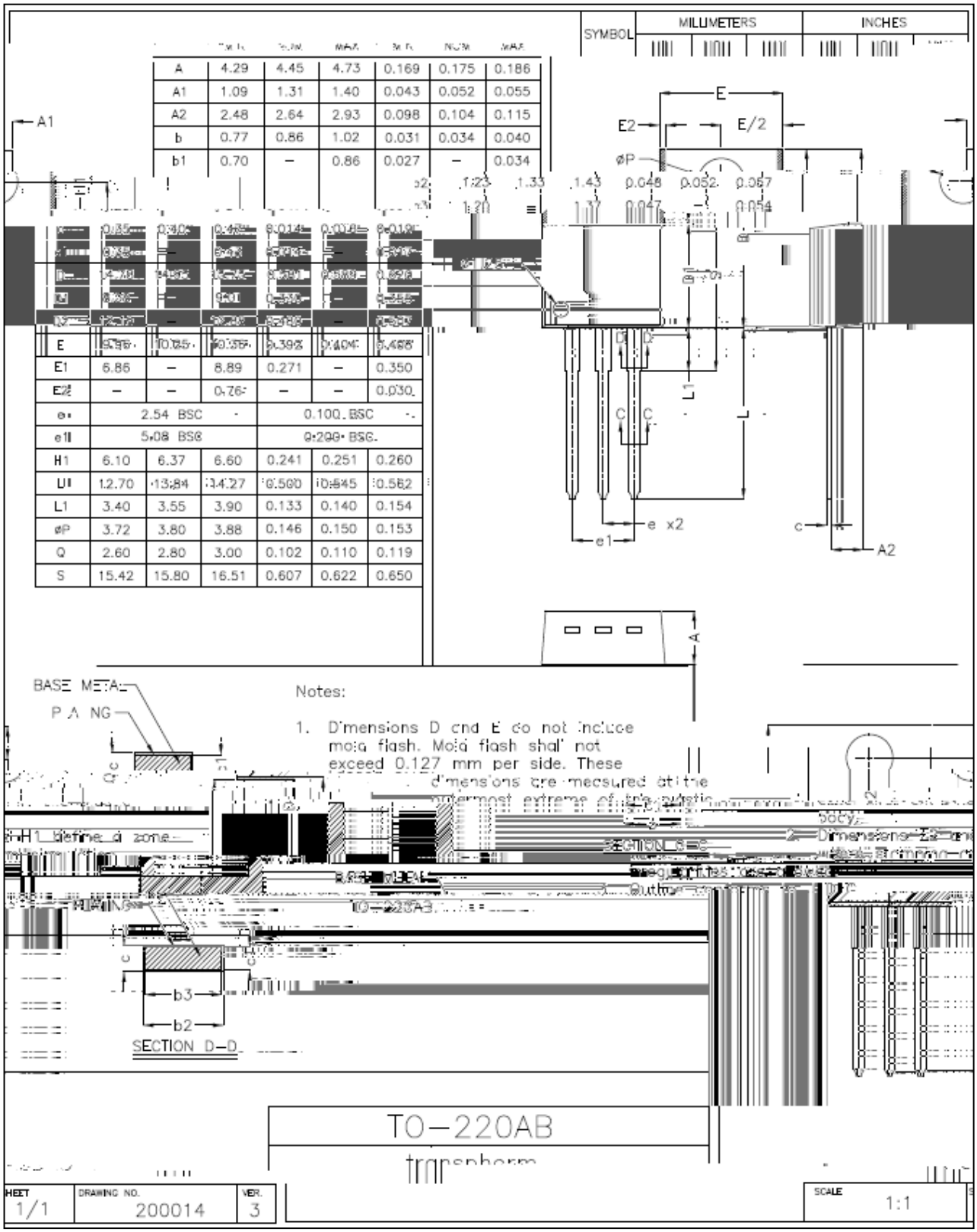


Figure 19. TO-220 Package Outline Drawing

6. Related Information

All technical documents for Renesas GaN Power devices are accessible from the GaN Power Solutions page.

7. Ordering Information

Part Number	Package Description	Package Configuration
TP65H150G4PS	TO220	Source

8. Revision History

Revision	Date	Description
3.00	Nov 25, 2025	

Corporate Headquarters

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Contact Information